REMARKS

Claims 1-18 are pending in the present application.

Request for Personal Interview

As discussed during the telephone interview with Examiner Phan on August 17, 2006, Applicant respectfully requests that a personal interview be granted prior to examination of this application responsive to this Request for Reconsideration, and that Supervisor Zarabian attends the personal interview.

Drawings

The drawings have been objected to in the Final Office Action dated February 22, 2006, as allegedly failing to comply with 37 C.F.R. 1.84(p)(4) for the various reasons given on page 2.

In the Advisory Action dated August 4, 2006, the Examiner has apparently acknowledged that the objection to the drawings under 35 C.F.R. 1.84(p)(4) has been withdrawn in view of the telephone interview conducted on July 18, 2006. The Examiner has acknowledged that "VDD" and "Vpp" are understandable in view of Fig. 3 as described in line 4, page 6; and lines 3, 6 and 22 of page 7 of the specification.

The drawings have also been objected to under 37 C.F.R. 1.83(a) beginning on page 2 of the Final Office Action, as allegedly failing to show every feature of the

invention specified in the claims. In the Advisory Action dated August 4, 2006, the Examiner has asserted:

1) that all Figs. 1-7 fail to show the connective relationship of the data line, the first bit line, the first sense amplifier, and the second sense amplifier in such a manner as recited in claims 1, 3, 4, 8, 9 and 13; and

2) that Fig. 7 only shows waveform TGR(L) at higher Vpp level at time t1 and then at lower VDD level, which is allegedly opposite to claims 7 and 17, which recite that the second voltage is higher than the first voltage.

This objection is respectfully traversed for the following reasons.

Regarding the first issue raised by the Examiner under 37 C.F.R. 1.83(a) as noted above, the Examiner's attention is respectfully directed to claim 1. The following comments are offered merely as an example to further the Examiner's understanding, and thus should not be construed as limiting.

As would be understood by anyone of ordinary skill in the art, Fig. 3 illustrates sense amplifier block 110 and control block 111. As shown in Fig. 2, the memory cell array includes a plurality of cell blocks 19 each including a sense amplifier block 110 and a control block 111. That is, a plurality of sense amplifier blocks 110 and control blocks 111 are shown as sequentially implemented in a vertical (column) direction in the memory cell array. In other words, sense amplifier block 110 and control block 111 in Fig. 3 of the present application can be considered as repetitively implemented in a

vertical (column) direction, wherein data buses DB and DBb extend in the vertical direction as coupled to each sense amplifier block 110 and control block 111 of a particular column. Incidentally, each sense amplifier block 110 inherently would include a respectively different sense amplifier coupled to respectively different bit line pairs BL and BLb.

Turning to claim 1, as described on page 8, lines 2-7 of the specification as originally filed, transistors 222 and 223 are turned on, and data bus DB and DBb are connected to a "first" sense amplifier 301 in response to the "H" level of column selecting signal Y[i]. The "first" sense amplifier 301 at this time is disconnected from bit line pair BL and BLb by transfer gates 302 and 303. The data is thus transferred from data bus DB and DBb to input nodes SBL and SBLb of "first" sense amplifier 301 while the "first" sense amplifier 301 is disconnected from bit line pair BL and BLb. This may be interpreted as readable on the first paragraph of claim 1.

As subsequently described on page 8, lines 6-12 of the original specification, thereafter the TGR signal is changed to the "H" level, and the "first" sense amplifier 301 is connected to bit line pair BL and BLb. Concurrently, it may be understood in view of Fig. 4, column selecting signal Y[i] is switched to the "L" level, disconnecting data bus DB and DBb from "first" sense amplifier 301. This may be interpreted as readable on the second paragraph of claim 1.

As subsequently described beginning on page 8, line 17 of the original

specification, in response to the "H" level of block selecting signal YBSEL[1] and column selecting signal Y[j], **another** or "second" sense amplifier 301 in **another** memory cell block 19 starts latching next data. As specifically described in the sentence bridging pages 8 and 9, the latching operation in the another sense amplifier 301 is started while the writing operation from sense amplifier 301 to the bit line pair BL and BLb is performed. This may be interpreted as readable on the third paragraph of claim 1.

Accordingly, Applicant respectfully submits that one of ordinary skill would readily understand that the drawings, taken in light of the description in the specification, do indeed show all the features of claim 1. With regard to claim 1, the drawings are thus in compliance with 37 C.F.R. 1.83(a).

During the telephone interview conducted on August 17, 2006, the Examiner raised concerns about how the embodiment of Fig. 3 operates. **If it is the Examiner's opinion that the embodiment of Fig. 3 can not operate as described, the Examiner is respectfully requested to clearly detail on the record the reasons why.** Applicant notes that this would not be an issue properly addressed under 37 C.F.R. 1.83(a).

In view of the above noted discussion, it is Applicant's position that the features 3, 4, 8, 9 and 13 should also be clearly evident in the drawings taken in light of the description in the specification. Regarding the last paragraph of claim 13, as noted

above, the sentence bridging pages 8 and 9 of the original specification describes that the latching operation in the another "second" sense amplifier is started while the writing operation from the "first" sense amplifier is performed, and that these operations thus clearly overlap.

Applicant thus respectfully submits that the first aspect of the objection to the drawings under 37 C.F.R. 1.83(a) as asserted in the Advisory Action should be considered as overcome in view of the above noted comments.

Regarding the second aspect of the objection to the drawings under 37 C.F.R. 1.83(a) as asserted in the Advisory Action, claim 7 features that the first bit line is connected to the first sense amplifier via a switching transistor, and "the switching transistor is driven by a first voltage and then driven by a second voltage which is higher than the first voltage". The following comments are offered with respect to this objection merely to further the Examiner's understanding, and thus should not be construed as limiting.

As described beginning on page 11, line 6 of the original specification with respect to Figs. 6 and 7, in response to the "L" level of column selecting signal Y[i], sense amplifier 301 is disconnected from data bus DB and DBb, and in response to the "H" level of signal TGR, sense amplifier 301 **is connected to** the bit line pair BL and BLb. As further described beginning on line 11 of page 11 of the original specification, in this operation when sense amplifier 301 is connected to bit line pair BL and BLb,

transistor 226 is driven by the voltage of VDD, which is shown as immediately subsequent time t_1 in Fig. 7. VDD may thus be interpreted as readable on the first voltage of claim 1.

As subsequently described beginning on page 11, line 14 of the original specification, after writing is completed, the array selecting signal XASEL has changed to the "L" level, and the power supply in the inverters 811 and 812 is changed to the Vpp level. Accordingly, transistor 226 is then driven by the Vpp level. This may be construed as occurring at the last transition of signal TGR(L) in Fig. 7, wherein the waveform transitions to the Vpp level. Thus, the Vpp level may be interpreted as the second voltage of claim 7.

Applicant respectfully submits that one of ordinary skill would readily understand that the drawings, taken in light of the specification, show the features of claim 7. **If it is the Examiner's opinion that Fig. 7 taken in light of the description does not show the features of claim 7, the Examiner is respectfully requested to clearly specify on the record the reasons why.**

Applicant further respectfully submits that in view of the above noted comments, the objection to the drawings under 37 C.F.R. 1.83(a) as set forth in the Final Office Action and as further addressed in the Advisory Action, should be overcome and thus withdrawn.